AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1. (Cancelled)

2. (Cancelled)

3. (Currently Amended) [[The]] An image processing apparatus ~~according to claim 2, further~~ comprising:

synchronous type processing means for carrying out a first image process on image data that is the subject of processing;

asynchronous type processing means for carrying out a second image process on a region of said image data that is the subject of processing;

synthesize means for synthesizing an output of said synchronous type processing means and an output of said asynchronous type processing means to form one image data, said synthesize means including:

a memory in which an output of said synchronous type processing means is stored, and

replacement means for replacing a portion of an output of said synchronous type processing means stored in said memory with an output of said asynchronous type processing means; and

control means for controlling replacement timing by said replacement means by detecting status of an output of said synchronous type processing means stored in said memory.

4. (Cancelled)

5. (Cancelled)

6. (Currently Amended) [[The]] An image processing apparatus ~~according to claim 5~~ comprising:

a first image processor formed of a hardware circuit, and carrying out a first image process on input image data;

a second image processor carrying out a second image process on a fragment of said input image data according to a program of predetermined software; and

a memory in which image data subjected to said first image process and image data subjected to said second image process are synthesized and stored,

wherein data of said memory in which image data subjected to the first image process is stored is overwritten by image data subjected to the second image process, and

wherein said second image processor detects a write timing of said image data subjected to the first image process into said memory to control a write timing into said memory.

7. (Previously Presented) The image processing apparatus according to claim [[4]] 6, wherein said software is rewritable.

8. (Currently Amended) [[The]] An image processing apparatus ~~according to claim 4,~~ comprising:

a first image processor formed of a hardware circuit, and carrying out a first image process on input image data;

a second image processor carrying out a second image process on a fragment of said input image data according to a program of predetermined software; and

a memory in which image data subjected to said first image process and image data subjected to said second image process are synthesized and stored,

wherein said second image processor detects a region on which the second image process is to be carried out by scanning input image data

9.-12. (Cancelled)

13. (Currently Amended) [[The]] An image processing apparatus ~~according to claim 12, further~~ comprising:

a synchronous type data processing device for carrying out a first image process on image data that is the subject of processing;

an asynchronous type data processor for carrying out a second image process on a region of said image data that is the subject of processing;

a data synthesizing device for synthesizing an output of said synchronous type processing device and an output of said asynchronous type processor to thereby form one image data, wherein said synthesizing device includes a memory for storing an output of said synchronous type processing device and said synthesizing device replaces a portion of an output of said synchronous type processing device stored in said memory with an output of said asynchronous type processor, and

a controller for controlling a replacement timing in said synthesizing device by detecting a status of an output of said synchronous-type processing device which is stored in said memory.